UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,799	10/30/2001	Chia-Lun Hang	DB000954-000	6066

24122 7590 03/20/2006

THORP REED & ARMSTRONG, LLP
ONE OXFORD CENTRE
301 GRANT STREET, 14TH FLOOR
PITTSBURGH, PA 15219-1425

EXAMINER	
ELMORE, REBA I	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 03/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,799	HANG, CHIA-LUN	
	Examiner	Art Unit	
	Reba I. Elmore	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,13-31 and 33-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11, 13-31 and 33-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 11, 13-31 and 33-58 are presented for examination.

DRAWINGS

2. The objection to the drawings is ***withdrawn*** due to the filing of new drawings March 25, 2005.

SPECIFICATION

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC 112, 1st paragraph

4. The rejection of claims 43-48 under 35 USC § 112, 1st paragraph is ***withdrawn*** due to the amendment.

35 USC § 102

5. The rejection of claims 1-36 as being anticipated by Nakamura is ***withdrawn***. All the claims are now rejected as being obvious under 35 USC § 103 as given below.

35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 11, 13-31 and 33-58 are rejected under 35 USC 103(a) as being unpatentable over Nakamura.

*****

8. Nakamura teaches the invention (claim 11) as claimed including a combination comprising:

an integrated circuit having a processor (e.g., see Figure 1, element 2);

an embedded memory array, the memory array having a plurality of controllers (e.g., see Figure 2, element 26) and a plurality of memory banks, each of the memory banks being independently connected to one of the plurality of controllers, each of the controllers being independently connected to the processor (e.g., see Figure 2 and paragraphs 0056-0061). Figure 2 shows each memory bank of the memory array has a memory controller, element 26;

a plurality of row address decoders, each of the row address decoders connected to one of the memory banks and one of he controllers as each memory bank having a separate row address decoder RDEC (e.g., see paragraph 0057); and,

a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controllers as each memory banks having a column address decoder CDEC with the controllers being equivalent to a command latch circuit within each memory bank (e.g., see paragraph 0057) such that the processor may communicate with the memory banks as a clock buffer (element 10, Figure 3) which in turn activates the plurality of address input buffers (e.g., see element 14, Figure 3), the plurality of command input buffers (e.g., see element 12, Figure 3) and data input buffers (e.g., see element 16a of Figure 3).

Nakamura does not specifically teach the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor

*****

because the necessary circuitry for this simultaneous access is shown in Figure 2 and paragraphs 0057-0062. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, the same clock pulse is sent to the plurality of memory banks allows this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 13, Nakamura teaches the memory array further comprises a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

As to claim 14, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see paragraphs 0057-0059).

As to claim 15, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see paragraphs 0057-0059).

As to claim 16, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of row address decoders and the plurality of column address decoders (e.g., see paragraphs 0057-0059).

As to claim 17, Nakamura teaches the embedded memory array is comprised of synchronous dynamic random access memory (e.g., see Figure 1 and paragraph 0053).

9. Nakamura teaches the invention (claim 18) as claimed comprising:

an integrated circuit having a processor (e.g., see Figure 1, element 2); and,

an embedded memory array, the memory array having a plurality of memory banks, each of the memory banks being connected to the processor independently of the connection of the other memory banks of the processor as each memory bank having its own connectivity including individual row decoders, column decoders and command latch circuitry (e.g., see Figure 2 and paragraphs 0056-0061).

*****

Nakamura does not specifically teach the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2 and paragraphs 0057-0062. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, the same clock pulse is sent to the plurality of memory banks allows this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 19, Nakamura teaches the memory array further comprises:

a plurality of controllers, each of the plurality of controllers being independently connected to the processor (e.g., see Figure 2);

a plurality of row address decoders, each of the row address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2); and,

a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2).

As to claim 20, Nakamura teaches the memory array has a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

As to claim 21, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see paragraphs 0057-0059).

As to claim 22, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see paragraphs 0057-0059).

*****

As to claim 23, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of controllers (e.g., see paragraphs 0057-0059).

As to claim 24, Nakamura teaches the embedded memory array is comprised of synchronous dynamic random access memory (e.g., see Figure 1 and paragraph 0053).

10. Nakamura teaches the invention (claim 25) as claimed including a combination, comprising:

a processor as the processing circuit (e.g., see Figure 1, element 2); and,

a plurality of transparent SDRAM arrays as embedded SDRAM (e.g., see paragraph 0053), each of the memory arrays having a plurality of memory banks being connected to the processor independently of the connection to the other memory banks to the processor as the memory banks having a plurality of row address decoders, each of the row address decoders connected to one of the memory banks and one of he controllers as each memory bank having a separate row address decoder RDEC (e.g., see paragraph 0057), a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controllers as each memory banks having a column address decoder CDEC with the controllers being equivalent to a command latch circuit within each memory bank (e.g., see paragraph 0057) such that the processor may communicate with the memory banks as a clock buffer (element 10, Figure 3) which in turn activates the plurality of address input buffers (e.g., see element 14, Figure 3), the plurality of command input buffers (e.g., see element 12, Figure 3) and data input buffers (e.g., see element 16a of Figure 3). The embedded SDRAM teaches the transparent memory array as a memory array which has a refresh operation for maintaining data in a power down mode without input from a programmer or system designer. The refresh operation is performed using a refresh address counter without supplying the address to the

*****

address buffer of the memory array for each cell of the array (e.g., see Figures 6-7 and paragraphs 0069-0077). Specifically, during an internal refresh, addresses and data are not supplied to the arrays, thereby using the refresh counter to supply the addresses needed for refreshing while in the low power mode and not row address signals and column address signals supplied by the address buffer. The direct connection between the processor and the embedded memory arrays is taught as the processor and memory arrays being on the same integrated circuit chip. The element labeled a 'memory controller' shown between the processor and the arrays supplies the same type of circuitry discussed by the Applicant as being necessary for the present invention. Simply labeling this circuitry 'memory controller' does not teach away from the direct connectivity. Nakamura does not show it being necessary for multiplexing between the processor and the memory arrays.

Nakamura does not specifically teach the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2 and paragraphs 0057-0062. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, the same clock pulse is sent to the plurality of memory banks allows this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 26, Nakamura teaches each of the plurality of transparent SDRAM memory arrays further comprises:

*****

a plurality of controllers, each of the plurality of controllers being independently connected to the processor and to one of the plurality of memory banks (e.g., see Figure 2);

a plurality of row address decoders, each of the row address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2); and,

a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2).

As to claim 27, Nakamura teaches the memory array has a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

As to claim 28, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 29, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 30, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of controllers (e.g., see Figure 1 and paragraph 0053).

11. Nakamura teaches the invention (claim 31) as claimed including a combination comprising:

a processor as the processing circuit (e.g., see Figure 1, element 2); and,

a plurality of transparent SDRAMs each having a plurality of memory banks, each of the plurality of memory banks being directly connected to the processor as embedded SDRAM. The embedded SDRAM teaches the transparent memory array as a memory array which has a refresh operation for maintaining data in a power down mode without input from a programmer or system designer. The refresh operation is performed using a refresh address counter without

*****

supplying the address to the address buffer of the memory array for each cell of the array (e.g., see Figures 6-7 and paragraphs 0069-0077). Specifically, during an internal refresh, addresses and data are not supplied to the arrays, thereby using the refresh counter to supply the addresses needed for refreshing while in the low power mode and not row address signals and column address signals supplied by the address buffer. The direct connection between the processor and the embedded memory arrays is taught as the processor and memory arrays being on the same integrated circuit chip. The element labeled a 'memory controller' shown between the processor and the arrays supplies the same type of circuitry discussed by the Applicant as being necessary for the present invention. Simply labeling this circuitry 'memory controller' does not teach away from the direct connectivity. Nakamura does not show it being necessary for multiplexing between the processor and the memory arrays;

a plurality of controllers with each of the controllers being independently connected to the processor and to one of the memory banks as each memory bank having controller circuitry (e.g., see element 2 of Figure 2);

a plurality of row address decoders with each of the row address decoders connected to one of the memory banks and one of he controllers as each memory bank having a separate row address decoder RDEC (e.g., see paragraph 0057 and Figure 2); and,

a plurality of column address decoders with each of the column address decoders being connected to one of the memory banks and to one of the controllers (e.g., see element 26, Figure 2) as each memory banks having a column address decoder CDEC such that the processor may communicate with the memory banks as a clock buffer (element 10, Figure 3) which in turn activates the plurality of address input buffers (e.g., see element 14, Figure 3), the plurality of command input buffers (e.g., see element 12, Figure 3) and data input buffers (e.g., see element 16a of Figure 3).

*****

Nakamura does not specifically teach the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2 and paragraphs 0057-0062. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, the same clock pulse is sent to the plurality of memory banks allows this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 33, Nakamura teaches the memory array has a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

As to claim 34, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 35, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 36, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of controllers (e.g., see Figure 1 and paragraph 0053).

12. Nakamura teaches the invention (claim 37) as claimed including a combination comprising:

a processor as the processing circuit (e.g., see Figure 1, element 2); and,

*****

a transparent SDRAM having a plurality of memory banks connected to the processor such that the processor access the memory banks as the SDRAM being embedded memory arrays.

Nakamura does not specifically teach the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2 and paragraphs 0057-0062. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, the same clock pulse is sent to the plurality of memory banks allows this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 38, Nakamura teaches each of the plurality of transparent SDRAM memory arrays further comprises:

a plurality of controllers, each of the plurality of controllers being independently connected to the processor and to one of the plurality of memory banks (e.g., see Figure 2);

a plurality of row address decoders, each of the row address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2); and,

a plurality of column address decoders, each of the column address decoders being connected to one of the memory banks and to one of the controllers (e.g., see Figure 2).

As to claim 39, Nakamura teaches the memory array has a data bus having a plurality of data lines, at least one of the plurality of data lines being connected to each of the memory banks (e.g., see Figure 2).

*****

As to claim 40, Nakamura teaches the data bus is operable to simultaneously receive data from each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 41, Nakamura teaches the data bus is operable to simultaneously provide data to each of the memory banks (e.g., see Figure 1 and paragraph 0053).

As to claim 42, Nakamura teaches the processor is operable to simultaneously send address information to more than one of the plurality of controllers (e.g., see Figure 1 and paragraph 0053).

13. Nakamura teaches the invention (claim 43) as claimed including a transparent memory array comprising:

a plurality of memory banks each comprised of a plurality of memory cells (e.g., see Figure 2);

a plurality of circuits for writing information into and reading information out of the memory cells, the plurality of circuits includes a plurality of controllers with control circuitry connected to each memory bank (e.g., see paragraphs 0057-0062 and Figure 2).

Nakamura does not specifically teach the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2 and paragraphs 0057-0062. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, the same clock pulse is sent to the plurality of memory banks allows this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

*****

As to claim 44, Nakamura teaches the plurality of circuits further comprises:

a plurality of row address decoders, each of the plurality of row address decoders having a row address input bus and a row address output bus, at least one of the plurality of row address decoders having the row address input bus connected to one of the plurality of controllers and having the row address output bus connected to one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060); and,

a plurality of column address decoders, each of the plurality of column address decoders having a column address input bus and a column address output bus at least one of the plurality of column address decoders having the column address input bus connected to at least one of the plurality of controllers and having the column address output bus connected to at least one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 45, Nakamura teaches the plurality of controllers are operable to exchange the address information and data with a processor (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 46, Nakamura teaches the plurality of controllers are operable to exchange the address information and data with the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 47, Nakamura teaches a data bus, the data bus having a plurality of data lines connected with each of the plurality of memory banks, the data bus operable to carry data signals from each of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 48, Nakamura teaches at least two of the memory arrays have a different data signal burst mode (e.g., see Figure 2 and paragraphs 0056-0060).

*****

14. Nakamura teaches the invention (claim 49) as claimed including a method for decreasing the access latency of an integrated circuit having a processor and a plurality of embedded memory arrays having a plurality of memory banks, the method comprising:

connecting each of the plurality of memory banks to the processor (e.g., see Figure 2 and paragraphs 0056-0060); and,

accessing the plurality of embedded memory banks with the processor (e.g., see Figure 2 and paragraphs 0056-0060).

Nakamura does not specifically teach the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2 and paragraphs 0057-0062. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, the same clock pulse is sent to the plurality of memory banks allows this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 50, Nakamura teaches the connecting step further comprises:

connecting each of the plurality of memory banks to one of a plurality of row address decoders, one of the plurality of row address decoders being connected to the processor(e.g., see Figure 2 and paragraphs 0056-0060); and,

connecting each of the plurality of memory banks to one of a plurality of column address decoders, one of the plurality of column address decoders being connected to the processor (e.g., see Figure 2 and paragraphs 0056-0060).

*****

As to claim 51, Nakamura teaches accessing step further comprises at least one of:

exchanging row address information between the processor and more than one of the plurality of row address decoders (e.g., see Figure 2 and paragraphs 0056-0060);

exchanging column address information between the processor and more than one of the plurality of column address decoders (e.g., see Figure 2 and paragraphs 0056-0060); and,

exchanging data between the processor and more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060).

Nakamura does not specifically teach the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2 and paragraphs 0057-0062. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, the same clock pulse is sent to the plurality of memory banks allows this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

15. Nakamura teaches the invention (claim 52) as claimed including a method for increasing the throughput of an integrated circuit having a processor and a transparent SDRAM array, the transparent SDRAM array having a controller, a data bus and a plurality of memory banks, each of the plurality of memory banks being independently connected to the controller, the method comprising at least one of:

reading data from more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0057-0062); and,

*****

writing data from more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0057-0062).

Nakamura does not specifically teach the processor simultaneously accesses more than one memory bank, however, Figure 2 shows each memory bank has an input buffer and an output buffer which indicates the simultaneous access is possible as well as each memory bank having separate circuitry. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have simultaneous access to the memory banks by the processor because the necessary circuitry for this simultaneous access is shown in Figure 2 and paragraphs 0057-0062. Even though the reference does not specifically state the memory banks can be accessed (read or write operations) simultaneously, the same clock pulse is sent to the plurality of memory banks allows this type of access is clearly implied by the figures and is thereby considered obvious in light of the drawings.

As to claim 53, Nakamura teaches the reading step further comprises:

exchanging read address information between the processor and more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060); and,

providing a data signal from the plurality of memory banks to the data bus (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 54, Nakamura teaches the writing step further comprises:

exchanging write address information between the processor and more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060); and,

providing a data signal from the plurality of memory banks to the data bus (e.g., see Figure 2 and paragraphs 0056-0060).

*****

As to claim 55, Nakamura teaches each of the memory banks has a row address decoder and a column address decoder associated therewith, the exchanging read address information step further comprises:

transmitting a first row address information from the processor to a first row address decoder (e.g., see Figure 2 and paragraphs 0056-0060);

transmitting a first column address information from the processor to a first column address decoder (e.g., see Figure 2 and paragraphs 0056-0060); and,

transmitting at least one of another row address information and column address information from the processor to at least one of another row address decoder and another column address decoder (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 56, Nakamura teaches providing a data signal from the plurality of memory banks to the data bus further comprises:

decoding the read address information exchanged between the processor and more than one of the memory banks (e.g., see Figure 2 and paragraphs 0056-0060);

selecting a memory cell within each of the memory banks based on the read address information (e.g., see Figure 2 and paragraphs 0056-0060); and,

read the data signal from the selected memory cells within the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 57, Nakamura teaches each of the memory banks has a row address decoder and a column address decoder associated therewith, the exchanging write address information step further comprises:

transmitting a first row address information from the processor to a first row address decoder (e.g., see Figure 2 and paragraphs 0056-0060);

*****

transmitting a first column address information from the processor to a first column address decoder (e.g., see Figure 2 and paragraphs 0056-0060); and,

transmitting at least one of another row address information and column address information from the processor to at least one of another row address decoder and another column address decoder (e.g., see Figure 2 and paragraphs 0056-0060).

As to claim 58, Nakamura teaches providing a data signal from the plurality of memory banks to the data bus further comprises:

decoding the write address information exchanged between the processor and more than one of the memory banks (e.g., see Figure 1 and paragraph 0053);

selecting a memory cell within each of the memory banks based on the write address information (e.g., see Figure 1 and paragraph 0053); and,

writing the data signal from the selected memory cells within the plurality of memory banks (e.g., see Figure 1 and paragraph 0053).

RESPONSE TO APPLICANT'S REMARKS

16. Applicant's arguments, see the remarks, filed December 9, 2005, with respect to the rejection(s) of claim(s) 1-58 under 35 USC § 102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the given interpretation of the claim language.

17. As to the reference teaching each memory bank having a command decoder, refresh address counter, address buffer, I/O buffer, command input buffer and clock input buffer which are common and not individual, this is not a valid interpretation of the Nakamura reference. Both Figure 3 and Figure 15 show there are a plurality of address input buffers and data input buffers. The reference also specifically states each memory bank has a row address decoder and column address decoder.

*****

18. As to the arguments that the processor may simultaneously communicate with more than one of the memory banks, this limitation is taught to the extent required by the actual claim language. The processor sends a clock signal which is the same signal provided by the clock input buffer to the buffers of the memory banks.

19. Additionally, the Applicant is arguing the specification of the present invention instead of the actual claim language

20. As to the processor not being independently connected to the memory banks because of commonly used elements, this is not a true interpretation of the reference since each memory bank has separate circuitry (e.g., see paragraph 0057).

21. As to arguments related to connectivity between the processor macro and the SDRAM macro being 'direct', the Applicant has provided only one definition of what is meant by this 'direct' connectivity in the present specification. This description states only that the connection is 'direct' due to the absence of multiplexing at the memory bank level of circuitry. Nakamura does not discuss a need for multiplexing but does state the logic macro and SDRAM macro are embedded on the same LSI (large scale integrated circuit). Connectivity on the same IC is considered 'direct' connectivity in the memory art. As to the reference not discussing the number of traces or circuit routings between components, the claims language is not this detailed. The limitations are taught by Nakamura to the extent required by the actual claim language.

22. As to the further arguments concerning 'simultaneous' access, the reference teaches this limitation to the extent required by the actual claim language. As stated previously, the reference does specifically teach circuitry associated with each memory bank. The reference does not explicitly teach the 'simultaneous' access by the processor, this concept is implicitly taught as each memory bank has separate circuitry which would allow such access.

*****

CONCLUSION

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on M-TH from 7:30am to 6:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2189

Monday, March 13, 2006

*****